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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,762	10/15/2003	Shiv Kumar Gupta	15164US01	6313

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EXAMINER	
GEBRESILASSIE, KIBROM K	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/685,762	GUPTA, SHIV KUMAR	
	Examiner	Art Unit	
	KIBROM GEBRESILASSIE	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,5 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,5 and 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to amended application filed on 09/28/2009.

2. Claims 4, 5, and 12 are presented for examination.

Response to Arguments

3. Applicant's argument relating to 102(f) rejection is not persuasive.

a. Applicants argued that "Specification 006 does not teach "a second circuitry configured to realize and verify the second on another chip while the first circuit verifies the first system on chip the second circuitry directly connected to the first circuitry". Secondly, it is noted that the claim limitation is in the past tense, "configured" as opposed to "configurable". Therefore, even if the emulator has the capacity, mere capacity is not configured".

Examiner respectfully disagrees. As applicant admitted, which stated as "many chip makers now use a device called a hardware emulator to verify SoCs, hardware emulator is a device with large amounts of logic and other circuitry as highly configurable connection, the connections can be configured so as to realize the design of the SOC, the hardware emulator has sufficient logic and circuitry to realize the design described in the data structure, the hardware emulator has sufficient capacity to realize the design (See: specification par [0006]). The underline section clearly indicates the hardware emulator comprises more than one circuitry which is configured to verify the SoCs.

4. Applicant's argument relating to art rejection is not persuasive.

b. Applicants argued that "emulator circuits 104, 108" are in fact, two emulator circuits. In contrast, Assignee claims "a hardware emulator for verifying" a first system on a chip and second system on another chip"-noting the use of the singular context in the claim" (Remarks, pg. 1 fourth paragraph).

Examiner respectfully disagrees. Rohfleisch et al discloses "the emulator circuits 104, 108 and the emulator interface circuits 110 permits an SOC designer or programmer to test, evaluate and/or debug the processor core 102 and other core 106 (i.e. first and second chips) using emulation interface circuits" (See: par [0039).

c. Applicants argued that Rohfleisch et al fails to disclose "a hardware emulator for verifying a first system on a chip and a second system on another chip, said hardware emulator comprising: a first circuitry configured to realize and verify the first system on chip, said first circuitry further comprising at least one output port for providing verification results from the first circuitry; and a second circuitry configured to realize and verify the second system on another chip while the first circuit verifies the first system on chip, the second circuitry directly connected to the first circuitry".

Examiner respectfully disagrees. The above recited limitation is analogous to the following teaching of the prior art:

"the emulator circuit 104 (i.e. first circuitry) is responsive to the control signals received over emulator control channel 114 from the emulation interface

circuit 110, the control signals cause the emulator circuit 104 to monitor processor core 102 (See: par [0030]),

the emulator circuit 108 (i.e. second circuitry) is responsive to the control signals received over emulator control channel from the emulation interface circuit 110, the emulator circuit 108 monitors other core 106 (See: par [0033]),

the data signals from both emulator circuit 104 and 108 are provided from emulator circuit 110 through port 120 as part of the I/O information (See: par [0036).

Further. Fig. 1 shows the connection between core 102 and other core 106 (i.e. first and second circuitries) through the interface circuitry 110.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(f) he did not himself invent the subject matter sought to be patented.

6. Claims 4, 5, and 12 are rejected under 35 U.S.C. 102(f) because the applicant did not invent the claimed subject matter.

d. Applicant's admission establishes that applicant has invented a system of using a hardware emulator for verifying a plurality of systems of the prior art. Applicants have not disclosed inventing a hardware emulator system. As such, any claims directed to a system that facilities this system must be regarded as being invented by another.

e. These rejection may be overcome by evidence that applicant has somehow transformed the hardware emulator system of the prior art by some specialization. As currently disclosed, however, applicants' system of verifying using a hardware emulator merely uses the existing feature of the prior art.

f. Evidence that hardware emulator anticipates the invention of claims 4, and 5 is found in applicant's admission as explicitly recited in the disclosure of the invention.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 4, 5 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Publication No. 2004/0019827 issued to Rohfleisch et al.

g. As per Claims 1-3, Canceled.

h. As per Claim 4, Rohfleisch et al discloses a system for verifying a plurality of systems on a plurality of chips (such as "testing and debugging of integrated circuits"; See: par [0001]), said system comprising:

a hardware emulator for verifying a first system on a chip and a second system on another chip (such as "the emulator circuits 104, 108 and the emulator interface circuits permits an SOC designer or programmer to test, evaluate

and/or debug the processor core 102 and other core 106 using emulation interface circuits"; See: par [0039]) said hardware emulator comprising:

a first circuitry configured to realize and verify the a first system on a chip, said first circuitry chip (such as "the emulator circuit 104 (i.e. first circuitry) is responsive to the control signals received over emulator control channel 114 from the emulation interface circuit 110, the control signals cause the emulator circuit 104 to monitor processor core 102 (See: par [0030]), further comprising at least one output port for providing verification results from the first circuitry system on the chip (such as "the data signals from both emulator circuit 104 and emulator circuit 108 are preferably provided from the emulation interface circuit 110 through port 120 as part of the I/O information"; See: par [0036]); and

a second circuitry configured to realize and verify the a second system on another chip while the first circuit verifies verifying the first system on chip the emulator circuit 108 (i.e. second circuitry) is responsive to the control signals received over emulator control channel from the emulation interface circuit 110, the emulator circuit 108 monitors other core 106 (See: par [0033]), the second circuitry directly connected to the first circuitry (See; the connection between emulator circuit 104 and emulator circuit 108 with emulator interface 110 of Fig. 1).

a. As per Claim 5, Rohfleisch et al discloses the system of claim 4, wherein the hardware emulator further comprises:

a first interface operable connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry (such as "emulator interface circuit 110 provides the emulation control signals over emulator control channel 114 and receives the data signals indicating the state or condition of the emulator circuit 104"; See: par [0028); and

a second interface operable connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry (such a "the emulator circuit 108 is preferably responsive to the control signals receive over emulator control channel 118 from the emulation interface circuit 110"; See: par [0033]).

i. As per Claim 6-11, Cancelled.

j. As per Claim 12, Rohfleisch et al discloses the system of claim 4, wherein verifying the plurality of systems further comprises detecting errors in the plurality of systems (such as "debugging of programs and operations of systems on-a-chip"; See; Abstract).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KIBROM GEBRESILASSIE whose telephone number is (571)272-8571. The examiner can normally be reached on Monday-Friday 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KIBROM GEBRESILASSIE/
Examiner, Art Unit 2128

/Hugh Jones/
Primary Examiner, Art Unit 2128